UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,197	11/21/2003	Peter Ledel Gammel	23-39-4-8	2988

8933 7590 02/10/2006

DUANE MORRIS, LLP
IP DEPARTMENT
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103-4196

EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,197	GAMMEL ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Request for Continued Examination (RCE) filed January 11, 2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 6-7, 13-14, 17-18 and 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kato (US 2004/0051120 A1).

In regard to claims 1 and 14, Kato teaches a metal-oxide-semiconductor device having a length and a width comprising: a semiconductor layer 14 of a first conductivity type; first and second source/drain regions 17 of a second conductivity type formed in the semiconductor layer 14 proximate an upper surface of the semiconductor layer 14 and spaced laterally apart relative to one another along the length of the device, the first and second source/drain regions 17 being formed in an active region of the device; a gate 7 formed above the semiconductor layer 14 proximate the upper surface of the semiconductor layer 14 and at least partially between the first and second source/drain

regions 17, the gate being configured such that a dimension of the gate, defined substantially parallel to the width of the device (Figure 1(a)), is configured to be substantially within the active region of the device; and an isolation structure 24 formed in the semiconductor layer 14, the isolation structure 24 being configured to substantially isolate one or more portions of the first source/drain region 17 from corresponding portions of the second source/drain region 17 (Figures 1(a)-1(b), page 3, paragraph [0049]-[0053]).

In regard to claims 2, 17 and 22, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

In regard to claims 6 and 18, Kato teaches the isolation structure 24 comprising at least one trench formed between at least the one or more portions of the first and second source/drain regions 17 (Figures 1(a)-1(b), page 3, paragraph [0049]-[0053]).

In regard to claim 7, Kato teaches at least one of the one or more portions of the first and second source/drain regions 17 comprising an end of the at least one of the first and second source/drain regions 17 along a dimension substantially orthogonal to the gate 7 (Figures 1(a)-1(b), page 3, paragraph [0049]-[0053]).

In regard to claim 13, Kato teaches the active region of the device being substantially defined within a thin insulating region 6 of the device (Figures 1(a)-1(b), page 3, paragraph [0049]-[0053]).

In regard to claim 21, Kato teaches an integrated circuit including at least one metal-oxide-semiconductor (MOS) device having a length and a width, the at least one MOS device comprising: a semiconductor layer 14 of a first conductivity type; first and second source/drain regions 17 of a second conductivity type formed in the semiconductor layer 14 proximate an upper surface of the semiconductor layer 14 and spaced laterally apart relative to one another along the length of the device, the first and second source/drain regions 17 being formed in an active region of the device; a gate formed above the semiconductor layer 14 proximate the upper surface of the semiconductor layer 14 and at least partially between the first and second source/drain regions, the gate being configured such that a dimension of the gate, defined substantially parallel to the width of the device, is confined to be substantially within the active region of the device; and an isolation structure 24 formed in the semiconductor layer 14, the isolation structure being configured to substantially isolate one or more portions of the first source/drain region 17 from corresponding portions of the second source/drain region 17 (Figures 1(a)-1(b), page 3, paragraph [0049]-[0053]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (US 2004/0051120 A1) as applied to claims 1-2, 6-7, 13-14, 17-18 and 21-22 above, and further in view of Yu (US 2003/0213971 A1).

Kato teaches all mentioned in the rejection above.

However, Kato fails to teach a gate comprising a polysilicon layer and a salicide layer formed on at least a portion of the polysilicon layer.

Yu teaches a gate 126 & 132 comprising a polysilicon layer and a salicide layer formed on at least a portion of the polysilicon layer (Figure 3A, pages 2-3, paragraphs [0039]-[0042]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the metal-oxide semiconductor device structure as taught by Kato with the metal-oxide semiconductor device having a gate comprising a polysilicon layer and a salicide layer formed on at least a portion of the polysilicon layer as taught by Yu to protect the device from damage caused by electrostatic discharge (page 2, paragraph [0020]).

Claims 3, 15 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (US 2004/0051120 A1) as applied to claims 1-2, 6-7, 13-14, 17-18 and 21-22 above, and further in view of Kwon et al. (US 2003/0058027 A1).

Kato teaches all mentioned in the rejection above.

However, Kato fails to teach the isolation structure comprising a guard ring formed in the semiconductor layer proximate the upper surface of the semiconductor

layer between at least the one or more portions of the first and second source/drain regions the guard ring being of the first conductivity type.

Kwon et al. teach an isolation structure FOX & GD comprising a guard ring GD formed in a semiconductor layer P-sub proximate an upper surface of the semiconductor layer P-sub between at least the one or more portions of the first and second source/drain regions S1, D1, S2, D2, S3 & D3, S4, D4, S5, D5, the guard ring GD being of the first conductivity type (Figures 8-9, pages 3-4, paragraphs [0040]-[0042]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the metal-oxide-semiconductor device structure as taught by Kato with the metal-oxide-semiconductor device having an isolation structure comprising a guard ring formed in the semiconductor layer proximate the upper surface of the semiconductor layer between at least the one or more portions of the first and second source/drain regions the guard ring being of the first conductivity type as taught by Kwon et al. to provide a semiconductor device capable of reducing the effect parasitic bipolar transistors (page 4, paragraph [0041]).

Claims 4-5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (US 2004/0051120 A1) and Kwon et al. (US 2003/0058027 A1) as applied to claims 3, 15 and 23 above, and further in view of Ohuchi et al. (3,886579).

Kato and Kwon et al. teach all mentioned in the rejection above.

However, Kato and Kwon et al. fail to teach an impurity concentration of a guard ring substantially matched to an impurity concentration of a semiconductor layer, wherein in the impurity concentration of the guard ring is in a range of 10^{18} to about 10^{19} atoms per cubic centimeter.

In regard to claims 4 and 16, Ohuchi et al. teach an impurity concentration of a guard ring 5 (Figure 2, column 5, lines 19-21) substantially matched to an impurity concentration of a semiconductor layer 3 (Figure 2, column 4, lines 4-7).

In regard to claim 5, Ohuchi et al. teach the impurity concentration of the guard ring 5 being 10^{19} - 10^{20} cm^{-3} (column 5, lines 19-20), which is in a range of 10^{18} to about 10^{19} atoms per cubic centimeter.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device structure as taught by Kato and the semiconductor device having an isolation structure comprising a guard ring formed in the semiconductor layer proximate the upper surface of the semiconductor layer between at least the one or more portions of the first and second source/drain regions the guard ring being of the first conductivity type as taught by Kwon et al. with the semiconductor device having an impurity concentration of a guard ring substantially matched to an impurity concentration of a semiconductor layer, wherein in the impurity concentration of the guard ring is in a range of 10^{18} to about 10^{19} atoms per cubic centimeter as taught by Ohuchi et al. to provide a semiconductor device capable of having a high response speed (column 2, lines 12-14 and 21-24).

Claims 9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (US 2004/0051120 A1) as applied to claims 1-2, 6-7, 13-14, 17-18 and 21-22 above, and further in view of Kwon et al. (US 2003/0058027 A1).

Kato teaches all mentioned in the rejection above.

However, Kato fails to teach the gate comprising a connection area for providing electrical connection to the gate, the connection area being proximate a middle portion of the gate along the dimension of the gate defined substantially parallel to at least one of the first and second source/drain region.

In regard to claims 9 and 20, Kwon et al. teach the gate 73/73', 74/74', 75/75' &76/76' comprising a connection area (connected to VDD) for providing electrical connection to the gate 73/73', 74/74', 75/75' &76/76', the connection area (connected to VDD) being proximate a middle portion of the gate 73/73', 74/74', 75/75' &76/76' along the dimension of the gate 73/73', 74/74', 75/75' &76/76' defined substantially parallel to at least one of the first and second source/drain region S1,S3,S3/D1,D2 & S4,S5/D3,D4,D5 (Figure 8, pages 3-4, paragraphs [0040]-[0041]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the metal-oxide-semiconductor device structure as taught by Kato with the metal-oxide-semiconductor device having at least one of the one or more portions of the first and second source/drain regions comprising an end of the at least one of the first and second source/drain regions along a dimension substantially orthogonal to the gate as taught by Kwon et al. to provide a

metal-oxide-semiconductor device that has a configuration of a protected output circuit page 3, paragraphs [0032] and [0039]).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (US 2004/0051120 A1) as applied to claims 1-2, 6-7, 13-14, 17-18 and 21-22 above, and further in view of Lai et al. (US 6,635,946 B2).

Kato teaches all mentioned in the rejection above.

However, Kato fails to teach the first source/drain region comprising a source of the device and the second source/drain region comprising a drain of the device.

Lai et al. teach a first source/drain region 114a comprising a source of the device and a second source/drain region 114b comprising a drain of the device (Figure 1E, columns 65-66, lines 1-5).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the metal-oxide-semiconductor device structure as taught by Kato with the metal-oxide-semiconductor device having a source/drain region comprising a source of the device and a second source/drain region comprising a drain of the device as taught by Lai et al. to form source and drain regions by conventional processes (column 3, lines 65-67).

Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (US 2004/0051120 A1) as applied to claims 1-2, 6-7, 13-14, 17-18 and 21-22 above, and further in view of Yang (US 6,306,711 B1).

Kato teaches all mentioned in the rejection above.

However, Kato fails to teach a device comprising a diffused MOS (DMSO)/laterally diffused MOS (LDMOS) device.

Yang teaches a device comprising a diffused MOS (DMSO)/laterally diffused MOS (LDMOS) device (Figure 4E, column 2, lines 49-52).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the metal-oxide-semiconductor device structure as taught by Kato with the metal-oxide-semiconductor device being a laterally diffused MOS (LDMOS) device as taught by Yang to provide a high voltage semiconductor device (column 2, lines 19-24 and 49-52).

Response to Arguments

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to metal-oxide-semiconductor devices having length and width:

Chatterjee et al. (6,015,992)

Chen et al. (US 2004/0072391 A1)

Lee (US 6,756,270 B2)

Nemati et al. (US 6,888,177 B1)

Shinkawata (US 2001/0015452 A1) Tran et al. (US 2005,0078534 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
February 3, 2006

Ida M. Soward
AU 2822